IN THE CLAIMS

1. (Currently amended) A method for programming a one time programmable memory, comprising the steps of:

obtaining an array of transistors; ~~and~~

programming at least one of said transistors using a hot carrier transistor aging technique to alter a characteristic of said at least one of said transistor, wherein the hot carrier aging technique comprises injection of carriers into a gate oxide, ~~and~~ wherein the injection of carriers causes at least one of[,] the creation of traps[,] and the filling of traps, and wherein said altered characteristic is a change in a threshold voltage of said at least one of said transistors; and

detecting said programmed at least one of said transistors by sensing said change in said threshold voltage of said at least one of said transistors;

wherein said detecting step comprises the steps of (i) raising a source terminal for each of said array of transistors to a positive potential, (ii) raising a gate terminal for all transistors along a selected row to a positive potential and (iii) detecting whether a drain voltage changes from a precharge voltage level to approximately a cell transistor threshold voltage below said positive gate terminal potential.

2. (Original) The method of claim 1, wherein said programming step further comprises the step of applying a stressful voltage to said at least one of said transistors to cause said hot carrier transistor aging.

3. (Cancelled)

4. (Currently amended) The method of claim [3] 1, wherein said programming step further comprising the step of applying a stressful voltage to a drain and a gate of said at least one of said transistors to cause said change in said threshold voltage of said of said at least one of said transistors.

5. (Cancelled)

6. (Cancelled)

7. (Currently amended) The method of claim 1, wherein the step of programming causes ~~said altered characteristic is~~ a change in a saturation current of said at least one of said transistors.

8. (Original) The method of claim 7, wherein said programming step further comprising the step of applying a stressful voltage to a source and a gate of said at least one of said transistors to cause said change in said saturation current of said of said at least one of said transistors.

9. (Original) The method of claim 7, further comprising the step of detecting said programmed at least one of said transistors by sensing said change in said saturation current of said at least one of said transistors.

10. (Currently amended) The method of claim 7, wherein said detecting step further comprises the steps of raising ~~the~~ a voltage on at least one column in said array of transistors to a positive potential; raising a gate terminal of each transistor in a selected row to a positive potential and evaluating a rate of voltage decay of at least one column in said array of transistors.

11. (Currently amended) A one time programmable memory, comprising:

an array of transistors, wherein at least one of said transistors is programmed using hot carrier transistor aging to alter a characteristic of said at least one of said transistor, wherein the hot carrier aging comprises injection of carriers into a gate oxide, ~~and~~ wherein the injection of carriers causes at least one of[,] the creation of traps[,] and the filling of traps, and wherein said altered characteristic is a change in a threshold voltage of said at least one of said transistors; and

a circuit for sensing said altered characteristic of said at least one of said transistor, wherein said circuit senses said change in said threshold voltage of said at least one of said transistors, and wherein said circuit (i) raises a source terminal for each of said array of transistors to a positive potential, (ii) raises a gate terminal for all transistors along a selected row to a positive potential and (iii) detects whether a drain voltage changes from a precharge voltage level to approximately a cell transistor threshold voltage below said positive gate potential.

12. (Original) The one time programmable memory of claim 11, wherein said at least one of said transistors is programmed by applying a stressful voltage to said at least one of said transistors to cause said hot carrier transistor aging.

13. (Cancelled)

14. (Currently amended) The one time programmable memory of claim [13] 11, wherein said at least one of said transistors is programmed by applying a stressful voltage to a drain and a gate of said at least one of said transistors to cause said change in said threshold voltage of said of said at least one of said transistors.

15. (Cancelled)

16. (Cancelled)

17. (Currently amended) The one time programmable memory of claim 11, wherein the programming of said at least one of said transistors causes ~~said altered characteristic is~~ a change in a saturation current of said at least one of said transistors.

18. (Original) The one time programmable memory of claim 17, wherein said at least one of said transistors is programmed by applying a stressful voltage to a source and a gate of

said at least one of said transistors to cause said change in said saturation current of said of said at least one of said transistors.

19. (Original) The one time programmable memory of claim 17, wherein said circuit senses said change in said saturation current of said at least one of said transistors.

20. (Original) The one time programmable memory of claim 17, wherein said circuit raises a voltage on at least one column in said array of transistors to a positive potential; raises a gate terminal of each transistor in a selected row to a positive potential and evaluates a rate of voltage decay of at least one column in said array of transistors.

21. (Currently amended) A one time programmable memory element, comprising

at least one transistor that is programmed using hot carrier transistor aging to alter a transistor characteristic, wherein the hot carrier aging comprises injection of carriers into a gate oxide, ~~and~~ wherein the injection of carriers causes at least one of[,] the creation of traps[,] and the filling of traps, and wherein said altered transistor characteristic is a change in a threshold voltage of said at least one transistor; and

a circuit for sensing said altered characteristic of said at least one transistor, wherein said circuit senses said change in said threshold voltage, and wherein said circuit (i) raises a source terminal for said at least one transistor to a positive potential, (ii) raises a gate terminal for said at least one transistor to a positive potential and (iii) detects whether a drain voltage changes from a precharge voltage level to approximately a cell transistor threshold voltage below said positive gate potential.

22. (Currently amended) The one time programmable memory element of claim 21, wherein the programming of said at least one transistor causes ~~said altered characteristic is~~ a change in a saturation current of said transistor.

23. (Cancelled)

24. (Cancelled)

25. (Cancelled)

26. (Cancelled)

27. (Currently amended) An integrated circuit, comprising:

a one time programmable memory, comprising

an array of transistors, wherein at least one of said transistors is programmed using hot carrier transistor aging to alter a characteristic of said at least one of said transistor, wherein the hot carrier aging comprises injection of carriers into a gate oxide, ~~and~~ wherein the injection of carriers causes at least one of[,] the creation of traps[,] and the filling of traps, and wherein said altered characteristic is a change in a threshold voltage of said at least one of said transistors; and

a circuit for sensing said altered characteristic of said at least one of said transistor, wherein said circuit senses said change in said threshold voltage of said at least one of said transistors, and wherein said circuit (i) raises a source terminal for each of said array of transistors to a positive potential, (ii) raises a gate terminal for all transistors along a selected row to a positive potential and (iii) detects whether a drain voltage changes from a precharge voltage level to approximately a cell transistor threshold voltage below said positive gate potential.

28. (Original) The integrated circuit of claim 27, wherein said at least one of said transistors is programmed by applying a stressful voltage to said at least one of said transistors to cause said hot carrier transistor aging.

29. (Cancelled)

30. (Cancelled)

31. (Currently amended) The integrated circuit of claim 27, wherein the programming of said at least one transistor causes ~~said altered characteristic is~~ a change in a saturation current of said at least one of said transistors.